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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,165	10/28/2003	Sanh D. Tang	6047-64397	7628

7590 07/20/2004

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,165	TANG ET AL.	
	Examiner	Art Unit	
	Nema O Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 34-40 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 34-40 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10282003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 36 is objected to because of the following informalities: line 3 after "shallow-trench", insolated is misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 34-40 are rejected under 35 U.S.C. 102(a) as being anticipated by Manning (2001/0002056). Manning discloses a semiconductor device and method of forming electrical interconnects and buried bit lines in a semiconductor device comprising: providing a substrate (Figs.5-13 el.142) having two or more transistors with active areas therebetween (Fig.5); creating an insulating layer (el.202,230) overlying the transistors and active areas; forming a hard mask over the insulating layer (implied in para.31); patterning the hard mask to define cell contacts above the active areas and buried bit lines between the cell contacts (para.31); removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches (Fig.9); depositing spacers (Fig.10 el.232) to substantially fill the buried bit line trenches; removing portions of the insulating layer within the cell contact trenches to expose the active areas

underlying the cell contacts (Fig.9); recess the spacers within the buried bit lines (para.33); and deposit conductive material within the buried bit line trenches and the cell contact trenches (para.35; Fig.11) **[claims 34, 38]**.

Manning also discloses a semiconductor device and method of forming electrical interconnects and buried bit lines in a semiconductor device comprising: providing a substrate (Figs.5-13 el.142) having two or more FET transistors with active areas therebetween (Fig.5); creating an insulating layer (el.202,230) overlying the transistors and active areas; patterning the insulating layer to define cell contacts above the active areas and buried bit lines between the cell contacts (para.31); removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches (Fig.9); depositing dielectric material to form spacers (Fig.10 el.232) within the buried bit line trenches and a dielectric layer within the cell contact trenches; removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts (Fig.9) while recessing the spacers within the buried bit lines (para.33); and depositing conductive material within the buried bit line trenches and the cell contact trenches (para.35; Fig.11) **[claims 35, 39]**.

Manning also discloses a semiconductor device and method of forming electrical interconnects and buried bit lines in a semiconductor device comprising: providing a substrate (Figs.5-13 el.142) having two or more shallow-trench isolated transistors with active areas therebetween and word lines traversing the active areas (para.28,26; Fig.5); creating an insulating layer (el.202,230) overlying the transistors, active areas and word lines; patterning the insulating layer to define cell contacts above the active

areas and buried bit lines above shallow trenches of the transistors (para.31); removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches (Fig.9); depositing dielectric material to form spacers (el.232) within the buried bit line trenches and a dielectric layer within the cell contact trenches (Fig.10); removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts (Fig.9) while partially removing the spacers within the buried bit lines (para.33); and depositing conductive material within the buried bit line trenches and the cell contact trenches (para.35; Fig.11) **[claims 36, 40]**.

Manning also discloses wherein the spacers comprise TEOS or silicon dioxide (para.33) **[claim 37]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Nema Berezny